100

150 — BUS MASTER STATE MACHINE

INT.

140 — COMMAND STATE MACH.

CMD

160 — MEMORY

COMMAND REG.

166 — CONFIG./ STATUS REG.

180 — INTER-FACE

CNTL

162

170 — STATUS & FEEDBACK CIRCUIT

LOOP COUNTER

LOOP TIMER

DATA LFSR

172   174   176

INT.

INTRPT GEN. — 190
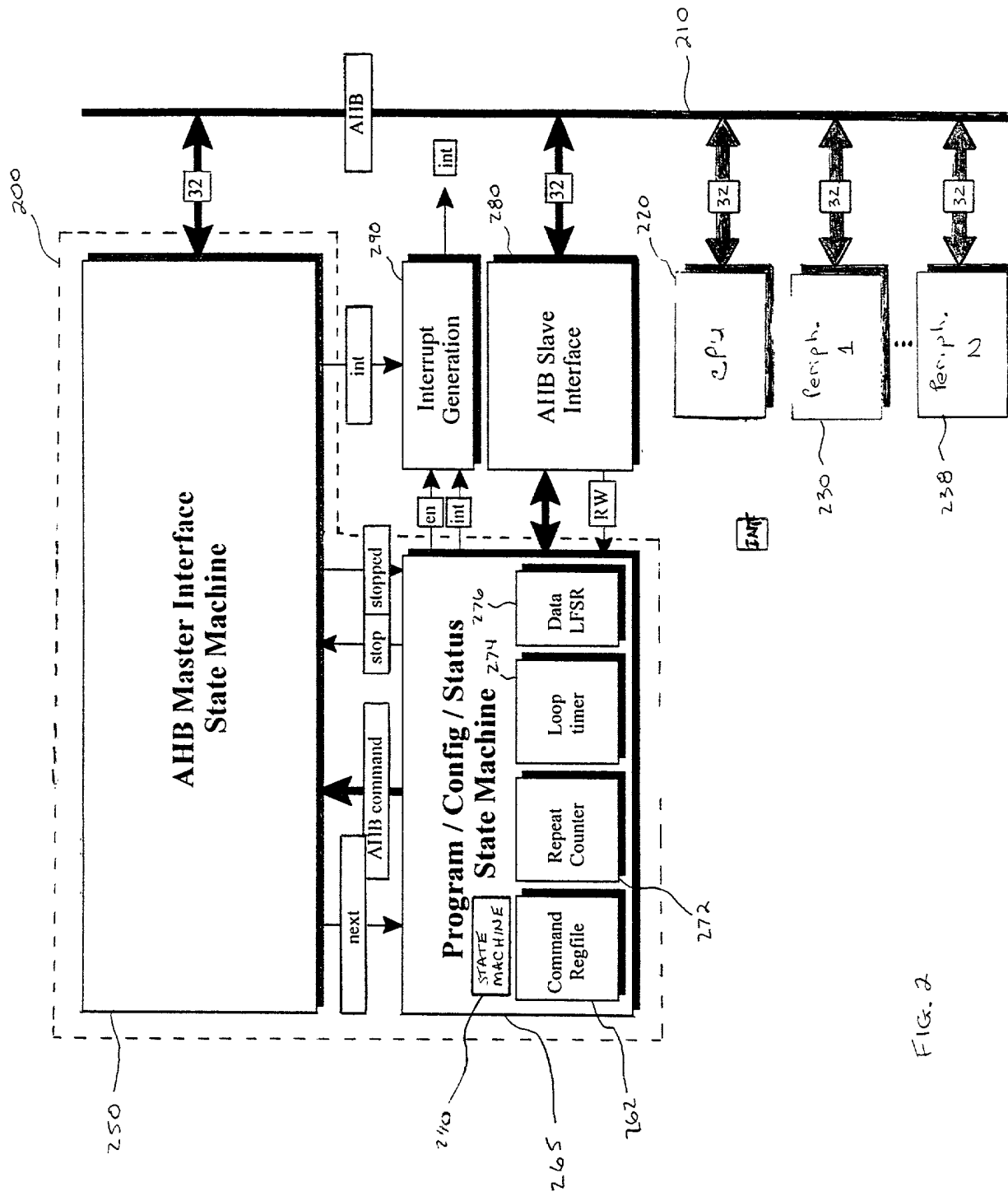
110

120

CPU

130 — Periph. 1

132 — Periph. 2

138 — Periph. N

FIG. 1

VLSI.323PA (780272)

AIIB

AHB Master Interface State Machine

Program / Config / Status State Machine

STATE MACHINE

next

AIIB command

stop stopped

Command Regfile

Repeat Counter

Loop timer

Data LFSR

en int

RW

Interrupt Generation

int

int

AIIB Slave Interface

32

32

CPU

Periph. 1

Periph. 2

32

32

32

INT

200

210

220

230

238

250

270

265

262

272

274

276

280

290

FIG. 2